What is claimed is:

1. A semiconductor device manufacturing method comprising the steps of:

(a) forming a first insulating film on a semiconductor substrate having a memory region where a memory device is to be formed and a logic region where a logic device is to be formed;

(b) forming, in said first insulating film, a first contact plug electrically connected to said semiconductor substrate in said memory region and having its top surface exposed from said first insulating film, and a second contact plug electrically connected to said semiconductor substrate in said logic region and having its top surface exposed from said first insulating film;

said first contact plug formed in said step (b) having a first conductive film and a first conductive barrier layer formed on a top end of said first contact plug;

(c) forming an MIM (Metal-Insulator-Metal) capacitor in contact with said first conductive barrier layer and forming a second insulating film, covering said MIM capacitor, on a top surface of the structure obtained by said step (b); and

(d) after said step (c), forming in said second insulating film a third contact plug in contact with said second contact plug;

said MIM capacitor formed in said step (c) having a lower electrode in contact with said first conductive barrier layer, an upper electrode, and a dielectric film interposed therebetween.

2. The semiconductor device manufacturing method according to claim 1,

wherein, in said step (b), a fourth contact plug is further formed, said fourth contact plug being electrically connected to said semiconductor substrate in said memory

region and having its top surface exposed from said first insulating film,

in said step (d), a fifth contact plug is further formed in said second insulating film, said fifth contact plug being in contact with said fourth contact plug, and

said fourth contact plug formed in said step (b) has a second conductive barrier layer in its top portion and a second conductive film in a remaining portion.

3. The semiconductor device manufacturing method according to claim 2, further comprising the step (e) of, before said step (a), forming first and second source/drain regions at a given distance from each other in an upper surface of said semiconductor substrate in said memory region and forming a gate structure on the upper surface of said semiconductor substrate between said first and second source/drain regions,

wherein, in said step (a), said first insulating film is formed on said semiconductor substrate to cover said gate structure,

in said step (b), said first and fourth contact plugs are formed to be electrically connected respectively to said first and second source/drain regions, and

in said step (d), said fifth contact plug is formed with its top surface exposed from said second insulating film,

and wherein said semiconductor device manufacturing method further comprises the step (f) of forming on said second insulating film, a bit line in contact with said fifth contact plug.

4. The semiconductor device manufacturing method according to claim 2,

wherein said second conductive film has a higher conductivity than said second conductive barrier layer, and

said step (d) comprises the steps of:

(d-1) forming, in said second insulating film, a first contact hole reaching said second conductive barrier layer;

(d-2) removing said second conductive barrier layer exposed by said step (d-1) to expose said second conductive film, thereby forming a recess in said first insulating film; and

(d-3) forming said fifth contact plug to fill said first contact hole and said recess communicating therewith.

5. The semiconductor device manufacturing method according to claim 4,

wherein said step (d) further comprises the step (d-4) of, before said step (d-1), forming on said second insulating film a resist having a given opening pattern,

in said step (d-1), said second insulating film is etched using said resist as a mask to form said first contact hole in said second insulating film, and

in said step (d-2), said second conductive barrier layer exposed by said step (d-1) is etched and removed using said resist used in said step (d-1) as a mask again, and using an etching gas different from an etching gas used in said step (d-1).

6. The semiconductor device manufacturing method according to claim 2,

wherein said second conductive film has a higher conductivity than said second conductive barrier layer, and

said step (d) comprises the steps of:

(d-1) forming a resist on said second insulating film;

(d-2) forming, in said resist, a first opening pattern in correspondence with the position of said fourth contact plug;

(d-3) etching said second insulating film using, as a mask, said resist having said first opening pattern, so as to form in said second insulating film, a first contact hole reaching said fourth contact plug; and

(d-4) forming said fifth contact plug to fill said first contact hole,

and wherein, in said step (d-2), said first opening pattern is formed in said resist in misalignment with said fourth contact plug, and

in said step (d-3), an over-etching is performed to said second insulating film so that said first contact hole extends into said first insulating film, thereby exposing said second conductive barrier layer and a side surface of said second conductive film.

7. The semiconductor device manufacturing method according to claim 2,

wherein said second conductive film has a higher conductivity than said second conductive barrier layer, and

said step (d) comprises the steps of:

(d-1) forming a resist on said second insulating film;

(d-2) forming, in said resist, a first opening pattern in correspondence with the position of said fourth contact plug;

(d-3) etching said second insulating film using, as a mask, said resist having said first opening pattern, so as to form in said second insulating film a first contact hole reaching said fourth contact plug; and

(d-4) forming said fifth contact plug to fill said first contact hole,

and wherein, in said step (d-2), said first opening pattern having a larger diameter than said fourth contact plug is formed in said resist, and

in said step (d-3), an over-etching is performed to said second insulating film so that said first contact hole extends into said first insulating film, thereby exposing said

second conductive barrier layer and a side surface of said second conductive film.

8. The semiconductor device manufacturing method according to claim 1, wherein said second contact plug formed in said step (b) has a second conductive barrier layer in its top portion and a second conductive film in a remaining portion.

9. The semiconductor device manufacturing method according to claim 8,

wherein said second conductive film has a higher conductivity than said second conductive barrier layer, and

said step (d) comprises the steps of:

(d-1) forming, in said second insulating film, a first contact hole reaching said second conductive barrier layer;

(d-2) removing said second conductive barrier layer exposed by said step (d-1) to expose said second conductive film, thereby forming a recess in said first insulating film; and

(d-3) forming said third contact plug to fill said first contact hole and said recess communicating therewith.

10. The semiconductor device manufacturing method according to claim 9,

wherein said step (d) further comprises the step (d-4) of, before said step (d-1), forming on said second insulating film a resist having a given opening pattern,

and wherein, in said step (d-1), said second insulating film is etched using said resist as a mask to form said first contact hole in said second insulating film, and

in said step (d-2), said second conductive barrier layer exposed by said step (d-1) is etched and removed using said resist used in said step (d-1) as a mask again, and

using an etching gas different from an etching gas used in said step (d-1).

11. The semiconductor device manufacturing method according to claim 8, wherein said second conductive film has a higher conductivity than said second conductive barrier layer, and

said step (d) comprises the steps of:

(d-1) forming a resist on said second insulating film;

(d-2) forming, in said resist, a first opening pattern in correspondence with the position of said second contact plug;

(d-3) etching said second insulating film using, as a mask, said resist having said first opening pattern, so as to form in said second insulating film, a first contact hole reaching said second contact plug; and

(d-4) forming said third contact plug to fill said first contact hole,

and wherein, in said step (d-2), said first opening pattern is formed in said resist in misalignment with said second contact plug, and

in said step (d-3), an over-etching is performed to said second insulating film so that said first contact hole extends into said first insulating film, thereby exposing said second conductive barrier layer and a side surface of said second conductive film.

12. The semiconductor device manufacturing method according to claim 8, wherein said second conductive film has a higher conductivity than said second conductive barrier layer, and

wherein said step (d) comprises the steps of:

(d-1) forming a resist on said second insulating film;

(d-2) forming, in said resist, a first opening pattern in correspondence with the

position of said second contact plug;

(d-3) etching said second insulating film using, as a mask, said resist having said first opening pattern, so as to form in said second insulating film, a first contact hole reaching said second contact plug; and

(d-4) forming said third contact plug to fill said first contact hole,

and wherein, in said step (d-2), said first opening pattern having a larger diameter than said second contact plug is formed in said resist, and

in said step (d-3), an over-etching is performed to said second insulating film so that said first contact hole extends into said first insulating film, thereby exposing said second conductive barrier layer and a side surface of said second conductive film.

13. The semiconductor device manufacturing method according to claim 7, wherein said step (d-3) exposes the entire periphery of said side surface of said second conductive film.

14. The semiconductor device manufacturing method according to claim 1, further comprising the step (e) of, before said step (a), forming first and second source/drain regions at a given distance from each other in an upper surface of said semiconductor substrate in said memory region and forming a gate structure on the upper surface of said semiconductor substrate between said first and second source/drain regions,

wherein, in said step (a), said first insulating film is formed on said semiconductor substrate to cover said gate structure,

in said step (b), said first contact plug is formed to be electrically connected to said first source/drain region, and a fourth contact plug is further formed, said fourth

contact plug being electrically connected to said second source/drain region and having its top surface exposed from said first insulating film,

in said step (d), a fifth contact plug is further formed in said second insulating film, said fifth contact plug being in contact with said fourth contact plug and having its top surface exposed from said second insulating film, and

said semiconductor device manufacturing method further comprises the step (f) of forming on said second insulating film a bit line in contact with said fifth contact plug.

15. A semiconductor device comprising:

a semiconductor substrate having a memory region where a memory device is formed and a logic region where a logic device is formed;

a first insulating film provided on said semiconductor substrate;

a first contact plug provided in said first insulating film with its top surface exposed from said first insulating film, and electrically connected to said semiconductor substrate in said memory region;

a second contact plug provided in said first insulating film with its top surface exposed from said first insulating film, and electrically connected to said semiconductor substrate in said logic region;

an MIM capacitor having a lower electrode, an upper electrode, and a dielectric film interposed therebetween, said lower electrode being in contact with the top surface of said first contact plug;

a second insulating film provided on said first insulating film and covering said MIM capacitor; and

a third contact plug provided in said second insulating film and in contact with said second contact plug;

said first contact plug having a first conductive barrier layer in its top portion and a first conductive film in a remaining portion;

said second contact plug having a second conductive barrier layer in its top portion and having, in a remaining portion, a second conductive film having a higher conductivity than said second conductive barrier layer;

said third contact plug extending into said first insulating film and being in contact with said second conductive barrier layer and a side surface of said second conductive film.

16. The semiconductor device according to claim 15, wherein said third contact plug is in contact with the entire periphery of said side surface of said second conductive film.

17. The semiconductor device according to claim 15, further comprising:

first and second source/drain regions formed at a given distance from each other in an upper surface of said semiconductor substrate in said memory region; and

a gate structure provided on the upper surface of said semiconductor substrate between said first and second source/drain regions,

wherein said first insulating film is provided on said semiconductor substrate and covers said gate structure, and

said first contact plug is electrically connected with said first source/drain region,

and wherein said semiconductor device further comprises:

a fourth contact plug provided in said first insulating film and having its top surface exposed from said first insulating film, said fourth contact plug being electrically

connected to said second source/drain region;

a fifth contact plug provided in said second insulating film and having its top surface exposed from said second insulating film, said fifth contact plug being in contact with said fourth contact plug; and

a bit line provided on said second insulating film and being in contact with said fifth contact plug.

18. A semiconductor device comprising:

a semiconductor substrate having a memory region where a memory device is formed and a logic region where a logic device is formed;

a first insulating film provided on said semiconductor substrate;

first and second contact plugs provided in said first insulating film with their respective top surfaces exposed from said first insulating film, and electrically connected to said semiconductor substrate in said memory region;

a third contact plug provided in said first insulating film with its top surface exposed from said first insulating film, and electrically connected to said semiconductor substrate in said logic region;

an MIM capacitor having a lower electrode, an upper electrode, and a dielectric film interposed therebetween, said lower electrode being in contact with the top surface of said first contact plug;

a second insulating film provided on said first insulating film and covering said MIM capacitor;

a fourth contact plug provided in said second insulating film and being in contact with said second contact plug; and

a fifth contact plug provided in said second insulating film and being in contact

with said third contact plug;

said first contact plug having a first conductive barrier layer in its top portion and a first conductive film in a remaining portion;

said second contact plug having a second conductive barrier layer in its top portion and having, in a remaining portion, a second conductive film having a higher conductivity than said second conductive barrier layer;

said fourth contact plug extending into said first insulating film and being in contact with said second conductive barrier layer and a side surface of said second conductive film.

19. The semiconductor device according to claim 18, wherein said fourth contact plug is in contact with the entire periphery of said side surface of said second conductive film.

20. The semiconductor device according to claim 18, further comprising:

first and second source/drain regions formed at a given distance from each other in an upper surface of said semiconductor substrate in said memory region; and

a gate structure provided on the upper surface of said semiconductor substrate between said first and second source/drain regions,

wherein said first insulating film is provided on said semiconductor substrate and covers said gate structure,

said first and second contact plugs are electrically connected respectively with said first and second source/drain regions,

said fourth contact plug has its top surface exposed from said second insulating film, and

said semiconductor device further comprises a bit line provided on said second insulating film and being in contact with said fourth contact plug.